WHAT IS CLAIMED IS:

1. A TFT display controller comprising:

a frame buffer operational to store TFT display data supplied from outside;

a timing controller;

a pixel pipe line (PPL) operational in response to signals generated by the timing controller to fetch and convert the TFT display data to a desired TFT display format; and

TFT display source/gate gate driver controls operational in response to signals generated by the timing controller to control representation of the TFT display data,

wherein the frame buffer, timing controller, PPL, and source/gate driver controls are integrated onto a single die,

wherein the PPL outputs fixed data independent from the TFT display data to the source/gate driver controls in response to signals generated by the timing controller.

2. The TFT display controller according to claim 1 wherein the timing controller switches the output of the TFT display data of the converted format from the PPL and the output of the fixed data in a constant cycle and a constant ratio of time.

3. The TFT display controller according to claim 2 wherein black is displayed based on the fixed data.

4. The TFT display controller according to claim 2 further comprising a means for determining a frequency for representation of the converted TFT display data on the TFT display, said frequency determining means including a programmable phase lock loop.

5. A TFT display controller comprising:

a frame buffer operational to store TFT display data supplied from outside;

a timing controller;

a pixel pipe line (PPL) operational in response to signals generated by the timing controller to fetch and convert the TFT display data to a desired TFT display format; and

TFT display source/gate gate driver controls operational in response to signals generated by the timing controller to control representation of the TFT display data,

wherein the frame buffer, timing controller, PPL, and source/gate driver controls are integrated onto a single die,

wherein said PPL can be switched by the timing controller between a mode for FSC-TFT display and a mode for non-FSC-TFT display.

6. The TFT display controller according to claim 2 wherein the constant cycle and the constant ratio of time are programmable.

7. The TFT display controller according to claim 2

further comprising a power management control (PMC) register for a plurality of power management modes, wherein the output of the TFT display data and the output of the fixed data are switched in a constant cycle and a constant ratio of time that are independent for each power management mode.

8. A TFT display controller comprising:

a programmable timing controller;

a programmable pixel pipe line (PPL) operational in response to signals generated by the programmable timing controller to fetch and convert the TFT display data to a desired TFT display format;

a programmable color light sequencer operational in response to signals generated by the programmable timing controller signals to control a TFT display back light source; and

programmable TFT display source/gate driver controls operational in response to signals generated by the programmable timing controller to control representation of the TFT display data converted by the PPL on a desired TFT display selected from the group consisting of a field sequential color TFT display and a non-field sequential color TFT display.

9. The TFT display controller according to claim 8 wherein the frame buffer, PPL, color light sequencer, programmable source/gate driver controls and programmable timing controller are integrated onto a single die.

10. The TFT display controller according to claim 8

further comprising a programmable phase lock loop responsive to data stored therein to determine a frequency for representation of the TFT display data converted by the PPL.

11. The TFT display controller according to claim 8 wherein the PPL comprises a plurality of parallel pixel pipes.

12. The TFT display controller according to claim 11 wherein the PPL further comprises white and black fixed color data registers.

13. The TFT display controller according to claim 12 wherein the PPL further comprises path select logic having a display raster setting (DRS) register, wherein data stored in the DRS register determines the desired TFT display format.

14. The TFT display controller according to claim 8 further comprising a power management control (PMC) register, wherein data stored in the PMC register determines an output frequency associated with a PLL such that the PLL controls PPL data paths to manage power consumption of the PPL.

15. The TFT display controller according to claim 8 wherein the programmable timing controller comprises field controls and sub-field controls operational to generate field and sub-field timing signals for the PPL and the back light.

16. A TFT display controller comprising:

means for storing TFT display data;

means for storing power management control data;

means for generating timing control signals;

means for fetching and converting the TFT display data to a desired TFT display format in response to the timing control signals;

means for controlling a TFT display back light in response to the timing control signals;

means responsive to the timing control signals for controlling representation of the converted TFT display data on a desired TFT display selected from the group consisting of a field sequential color TFT display and a non-field sequential color TFT display; and

means for determining a frequency for representation of the converted TFT display data in response to data stored in the means for storing power management control data,

wherein the TFT data storing means, timing control signal generating means, and means for fetching and converting the TFT display data to a desired TFT format are integrated on a single die.

17. The TFT display controller according to claim 16 wherein the means for fetching and converting the TFT display data to a desired TFT display format comprises a programmable pixel pipe line which includes white and black fixed color data registers.

18. The TFT display controller according to claim 16 wherein the means for determining a frequency for

representation of the converted TFT display data comprises a programmable phase lock loop.